

Design Digitaler Schaltkreise

Place and route 2

Asic and Detector Lab - IPE

Prof. Ivan Peric ivan.peric@kit.edu

Richard Leys richard.leys@kit.edu

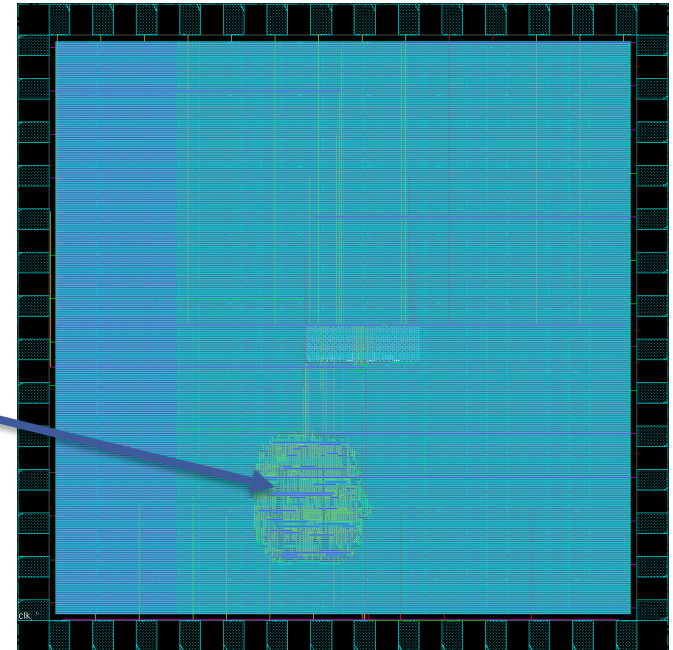


Lecture Goal

- Understand the basics of Timing Configuration
- Understand the concept of Clock Synthesis
- See last routing and design completion steps

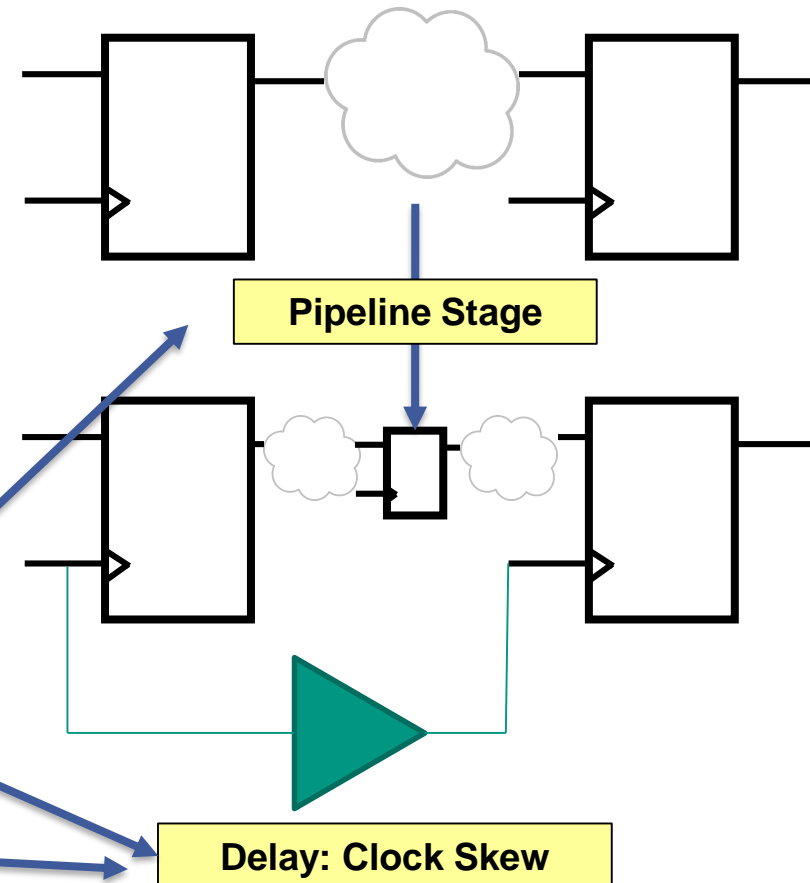
Where are we?

- Floorplaning is done and set
- Input Outputs are set
- Power structures have been planned
- Standard Cells are placed
- Remains:
 - Distribute the clock
 - Route the design
 - Respect Design Rules for manufacturing
 - Keep timing within acceptable margins
 - Output design data for DRC/LVS and production



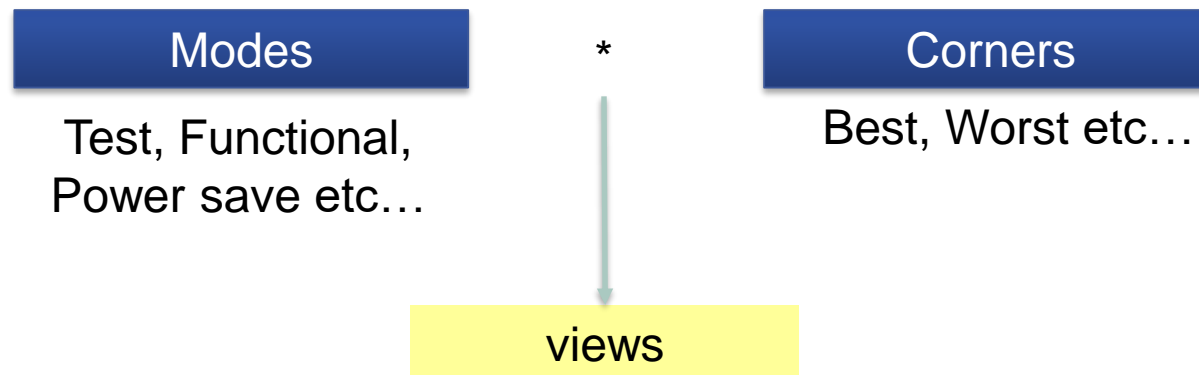
Reminder: Setup/Hold

- Clock Relation:
 - Setup: Time available before the next clock
 - Hold: Time “not available” after a clock cycle
- Slow / Fast:
 - Setup: Issue if we are too slow, not enough available time
 - Hold: Issue if we are too fast, not over the “unavailable” time
 - **Slow (setup) and Fast (hold) Corners required!!!**
- Implementation Fixes:
 - Setup:
 - Faster Logic -> Low VT Cells?
 - **Pipelining: Divide the logic in more clock periods**
 - Change Clock: Start next previous Flop-Flip later: Useful skew
 - Hold:
 - Slow the logic: Add delay Buffers
 - Change Clock: Start previous Flip-Flop clock later
- Post-Implementation Fixes:
 - Setup: Slow the clock...
 - Hold: Nothing to be done ☹



Timing Setup: MMMC

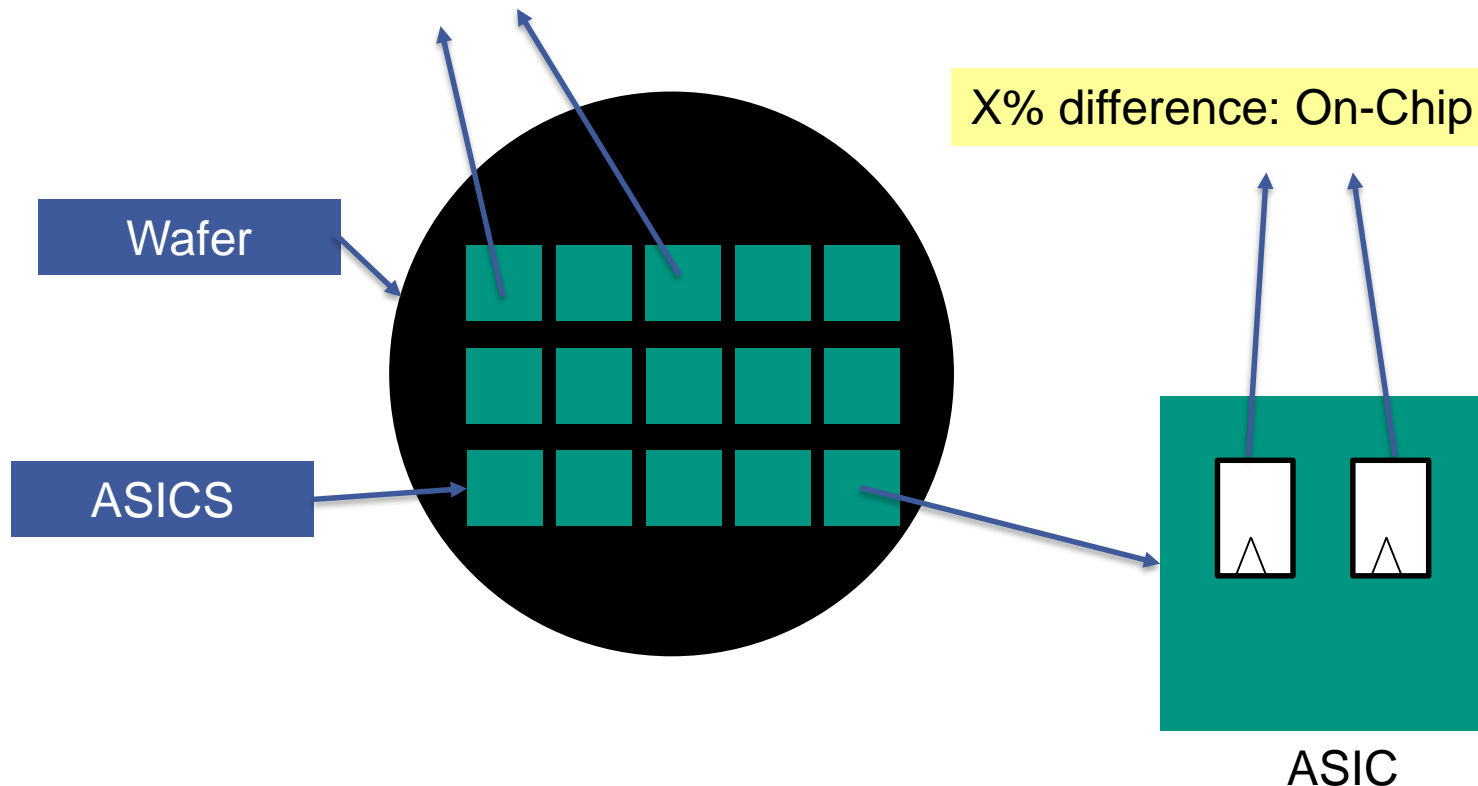
- Multi-Mode Multi-Corner
- Multi-Mode:
 - All configurations in which the ASIC can run, ex: Test mode, Functional
- Corners: Timing Characterisation of libraries for different conditions:
 - Voltages
 - Temperature
 - Best Case, Worst Case
- Views: Modes + Corners
 - Slow Corners: Fix Setup
 - Fast Corners: Fix Hold



Timing Setup: Process & On Chip Variation

■ OnChip Variation and Process/Temperature Variation

X% difference: Process Variation



Timing Setup: On Chip Variation

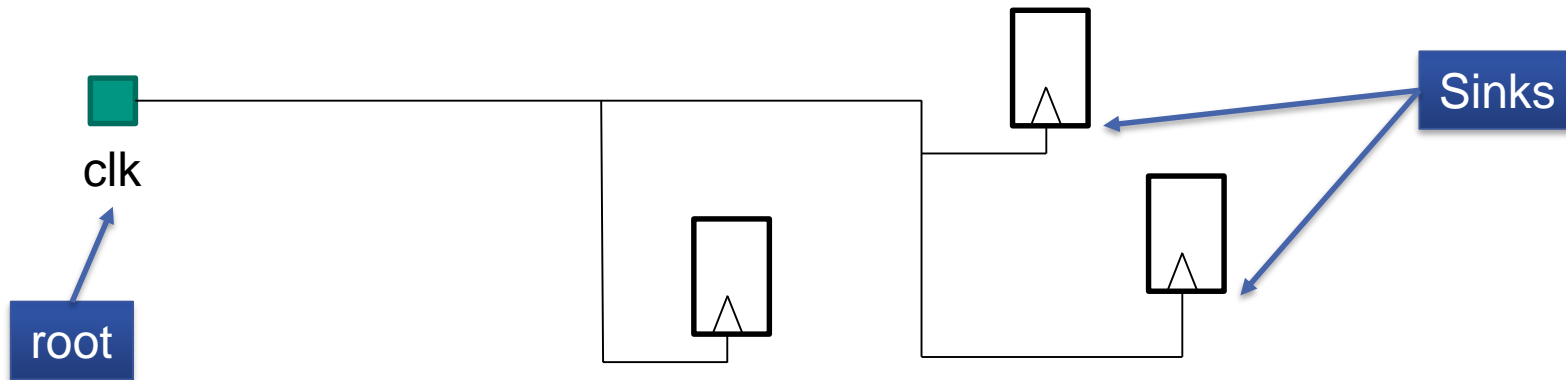
- For slower technology nodes ($<65\text{nm}$) On-Chip Variation (OCV) become more and more dominant:
 - Two adjacent transistors on the die are different.
 - The smaller the technology, the disparate it gets.
- OCV also affects RC extraction for routing lines
- OCV adds up as an extraction corner
 - Worsens the runtimes
- Setup challenges: Technology specific, not always easy to have correct values to setup the tool with.
- Difficulty for us: very much process-related, we are not process experts
- In an industry context: don't forget about it!

Timing Fixes during implementation

- In Cadence tools, the optDesign command is used to reclaim timing after each phase:
 - Before Clock Tree Synthesis
 - Before Routing
 - After Routing
- Timing Fixes are done for Setup and Hold separately
- Fixes may alter manufacturing rules (DRC)
- DRC may alter timing:
 - Always re-optimize the design along the implementation flow
- Ignore this right now:
 - No Specific pattern:
 - See what the tool does and re-call design optimisation with different options to fix alterations
 - Runtimes go higher, not a good idea for the lab work as well

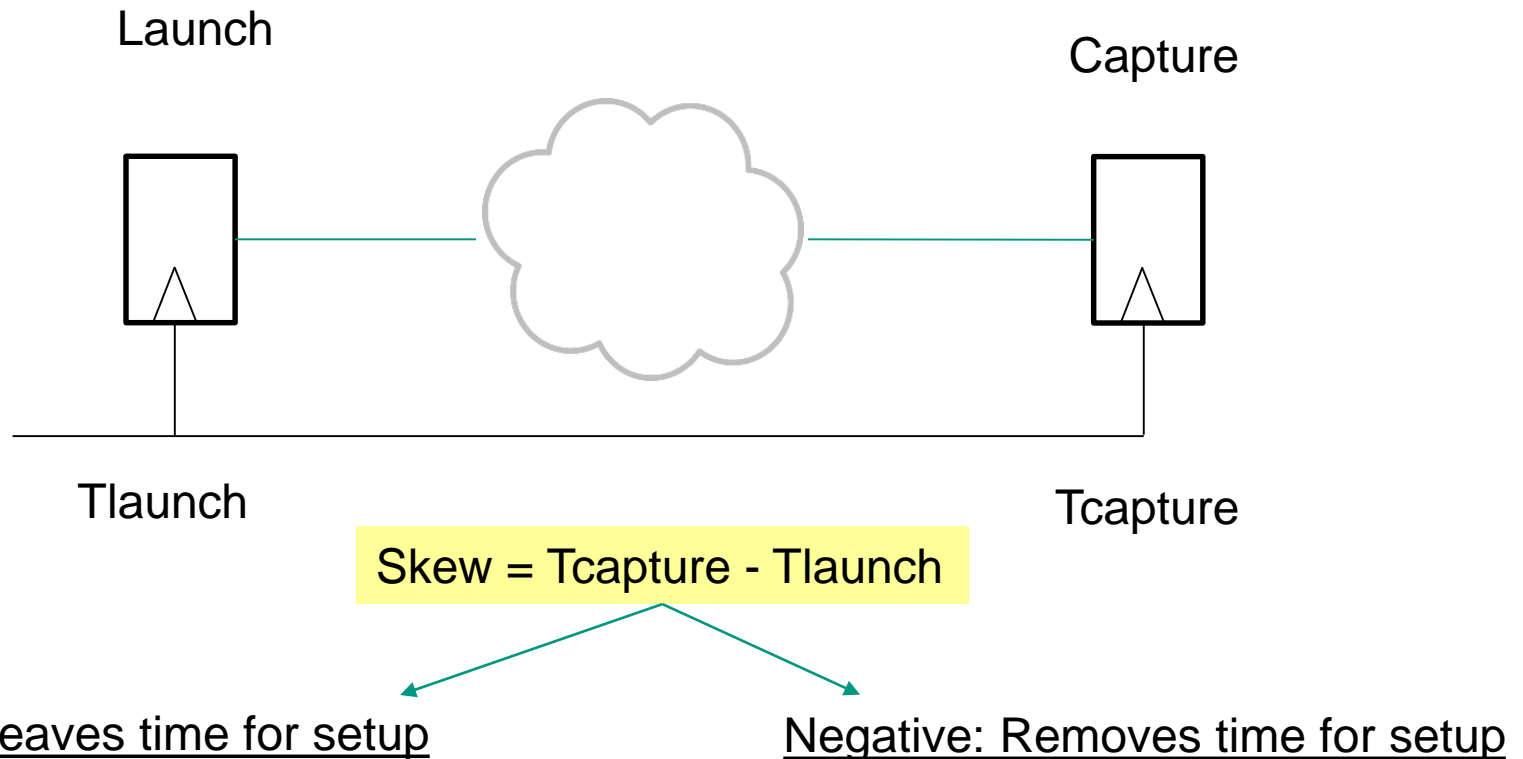
Clock Tree Synthesis (CTS)

- Per-Clock domain:
 - 1 Clock Source
 - Many Sinks
- Goal: Clock available at all flip-flops at the same time
- Clock net is very constraining:
 - Toggles a lot: Power consumption
 - Can toggle fast: Signal Integrity aggressor
 - Long wires: Difficult to drive and balance



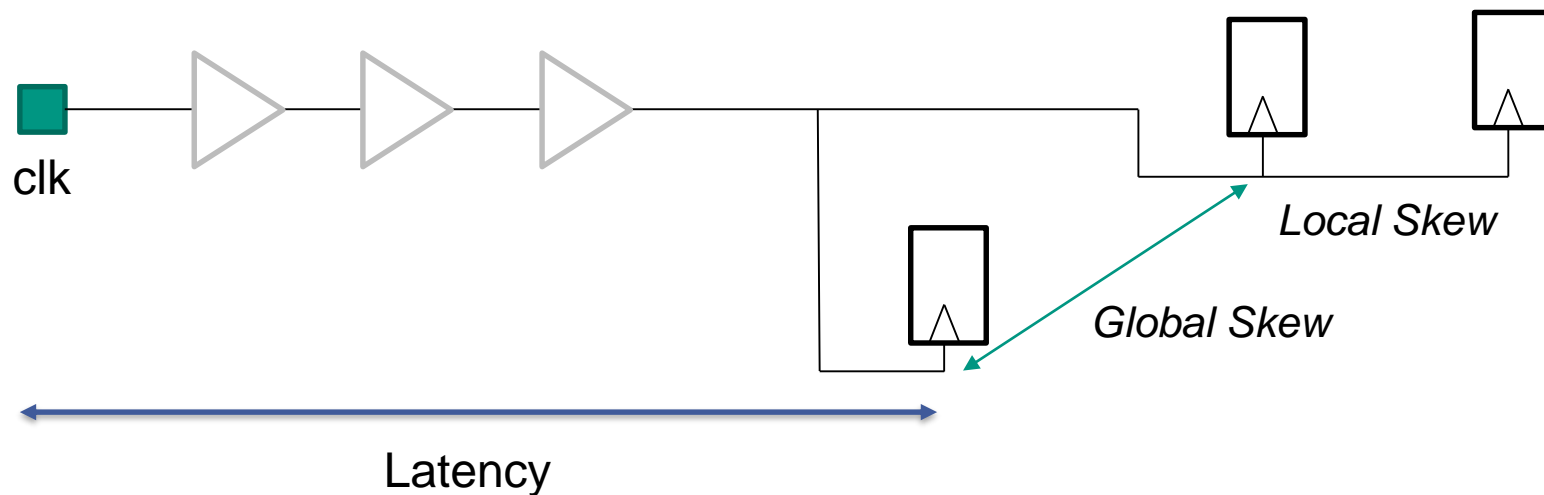
CTS: Clock Skew

- Clock arrives at Launch and Capture ports
- Positive and Negative Skew are possible



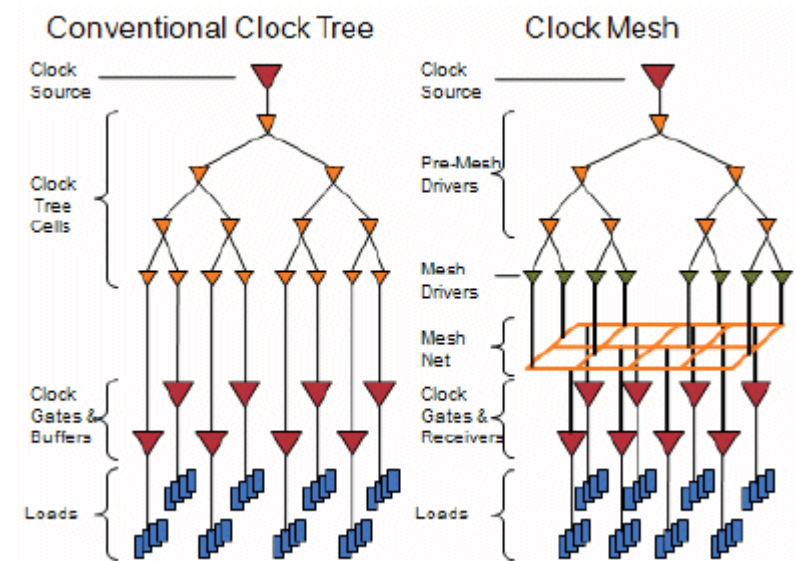
CTS: Semantics

- Latency is used to describe the time to reach the sinks
- Skew is defined in: Local and Global categories
 - Local for related flip-flops
 - Global for unrelated flip-flops



CTS: Achieving Zero-Skew

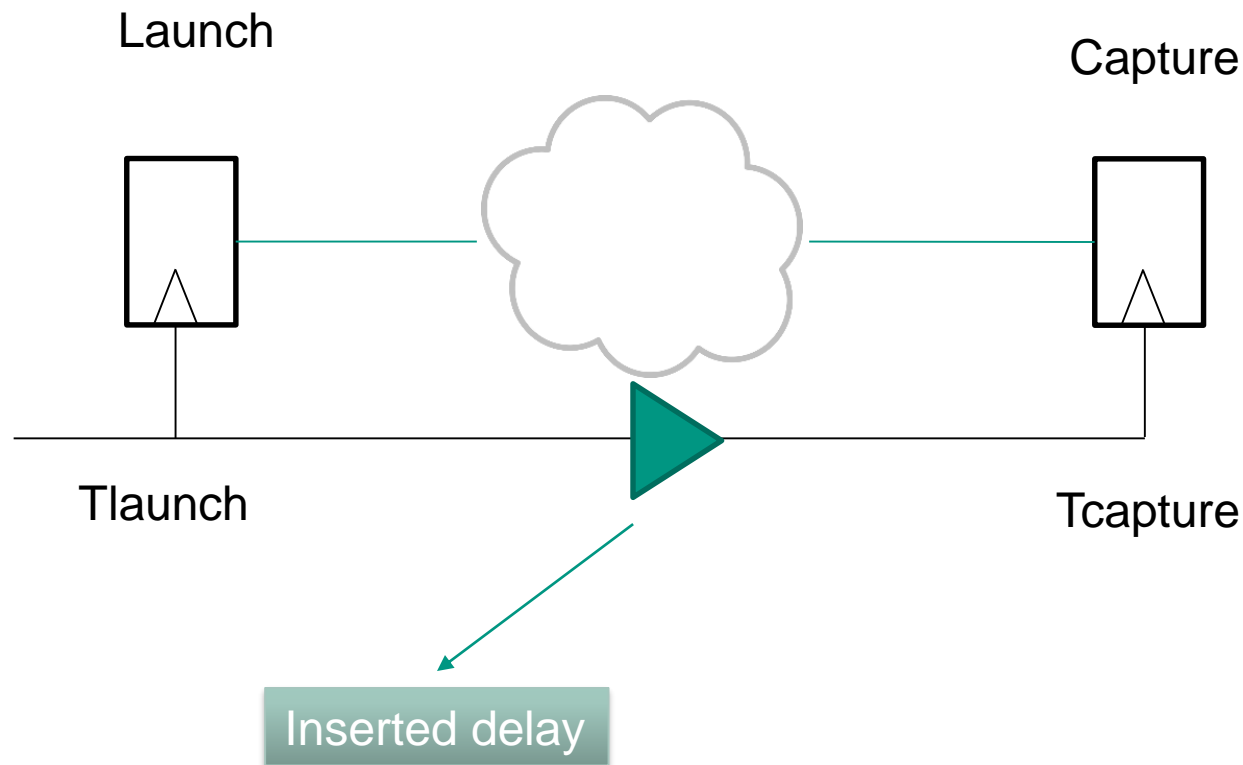
- There are two types of clock routing:
 - Clock Tree: The commonly used path
 - Clock mesh: A grid for the clock
 - Better Skew, but higher resource usage
- Main Goal: No skew
 - All flip-flops get the clock at the same time
- Zero-Skew clock tree algorithms are available and researched
 - Not the focus here
- At Lower technology nodes:
 - On-Chip Variation influence increases (OCV)
 - Clock meshes seem to have a better tolerance to OCV
- Rule: Understand what the tool can do, and the advantages for the specific technology and chip size



<http://www.design-reuse.com/articles/21019/clock-mesh-benefits-analysis.html>

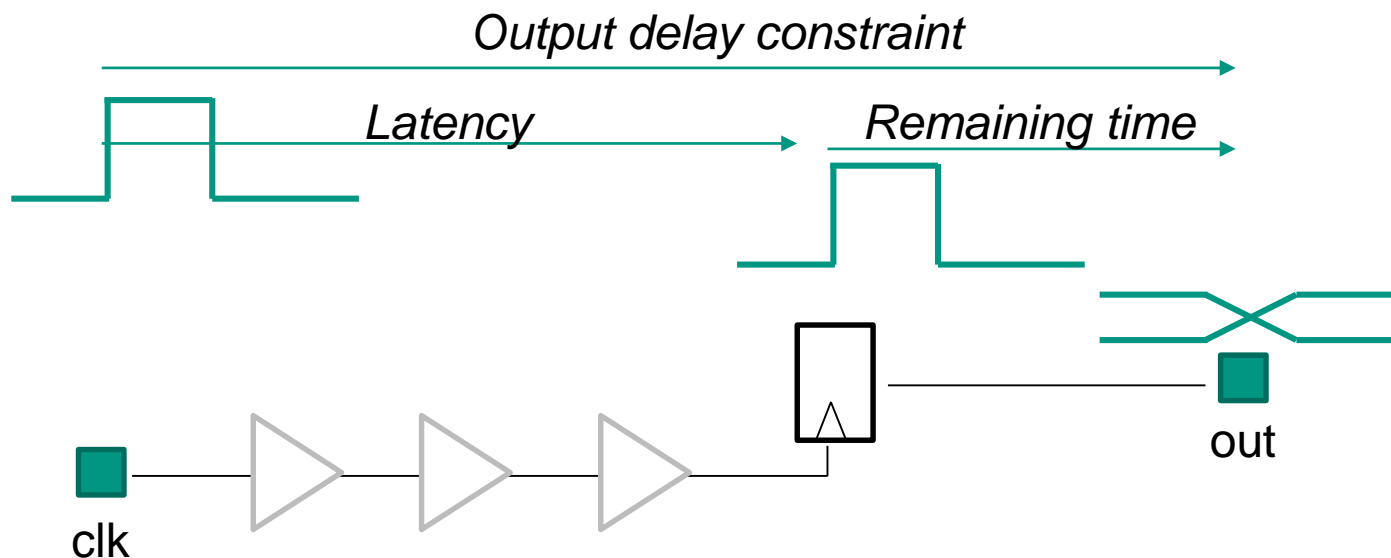
CTS: Useful Skew example

- Feature example: The tool can try to use positive/negative skew to improve setup or hold timing
- Use with precaution, first try to meet timing with no fancy feature

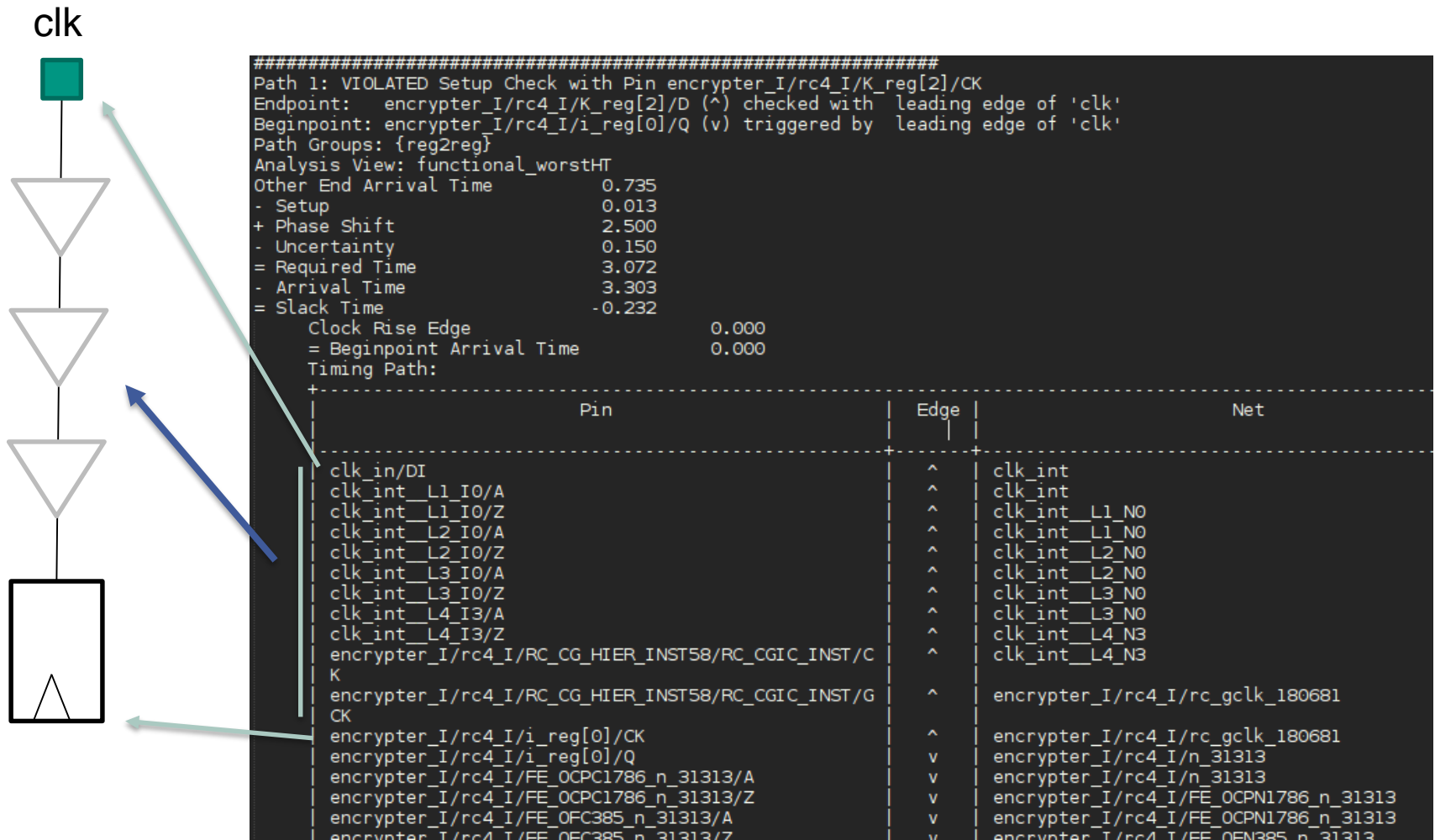


Clock Tree and IO Timing

- Clock Tree Latency usually shows up in timing violations for Input / Output Paths
- Reminder:
 - Input: Reserve time from clock period for signal to come to us
 - Output: Reserve time from clock period for signal to get to others
- Clock Tree Depth: Latency
- Latency adds time to clock: Good for input; bad for output

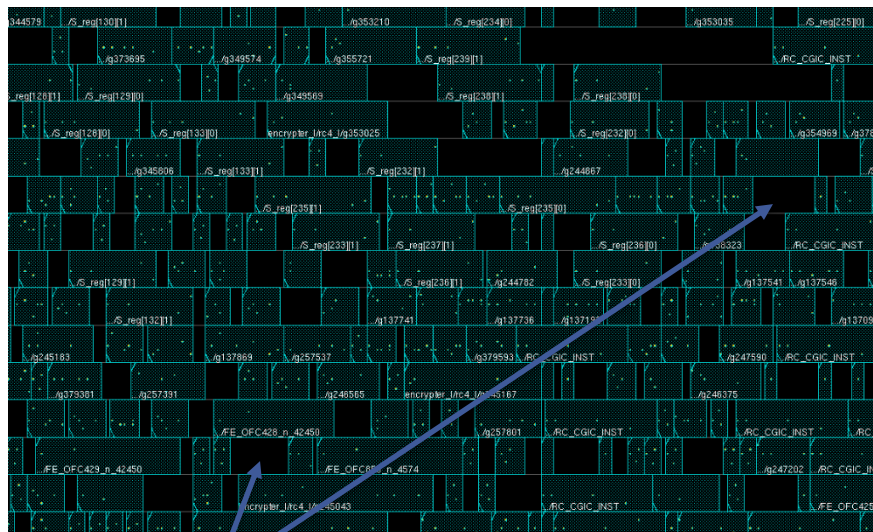


CTS: Report example

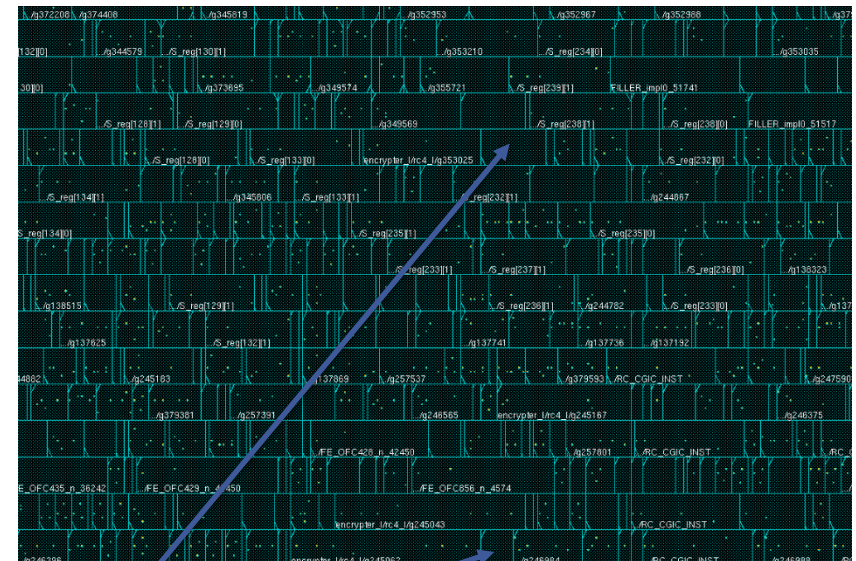


Routing: Global Overview

- Finish All data paths routing with accurate extraction
 - Fill the core area blanks with filler cells (see technology documentation for cell names)
 - Perform Global and detail routing
 - Extraction optimises RC and signal integrity quality
 - Timing is analysed and routing adapted in consequence



Blanks

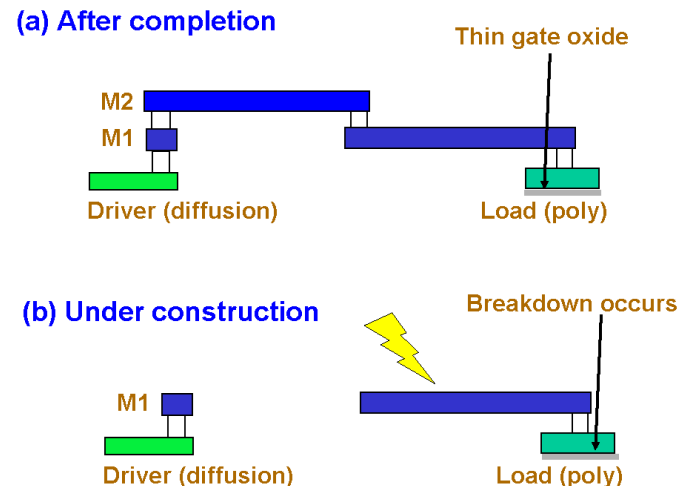


FILLERS

No Blanks

Routing: Antenna Fixing

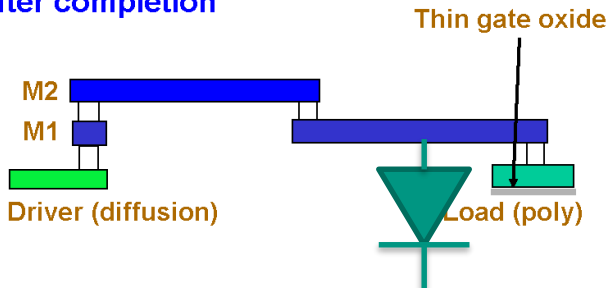
- Antenna is a risk during manufacturing process
 - A discharge may occur through routed floating nets to transistor gates
 - Charges Gather on metal during etching
 - IC would not be working if it happens
- Fixes:
 - Antenna Cells are inserted to ensure discharge occurs into substrate
 - Router can add « Layer Bridge »
- Routing might also leverage antenna fixing, so the router may route based on timing and Antenna constraints



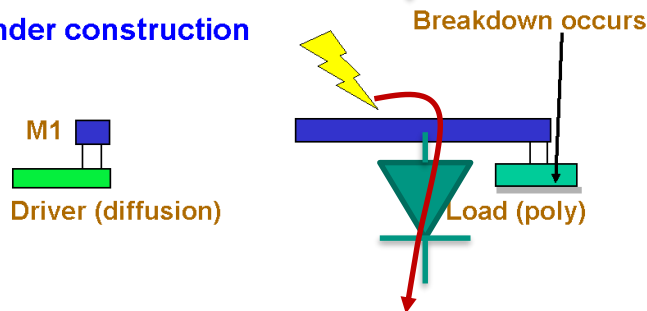
(wikipedia: Antenna Effect)

Routing: Antenna Fixing

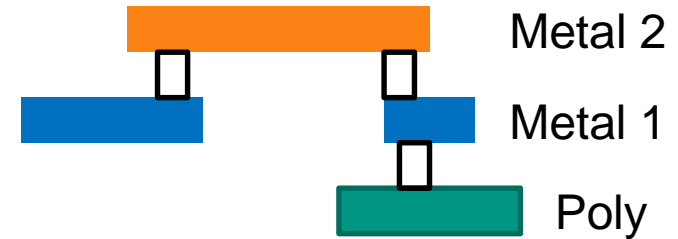
(a) After completion



(b) Under construction



Antenna FIX



Bridge Fix

- Metal 2 Build after Metal 1
- Metal 2 is Short

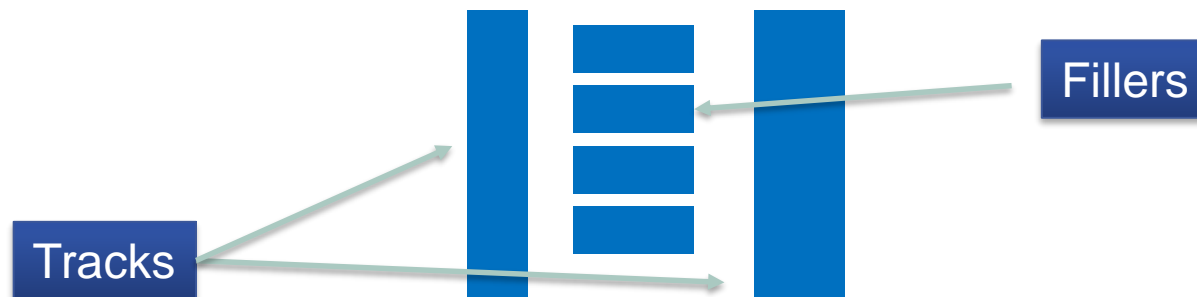
(wikipedia: Antenna Effect)

Prepare for Manufacturing

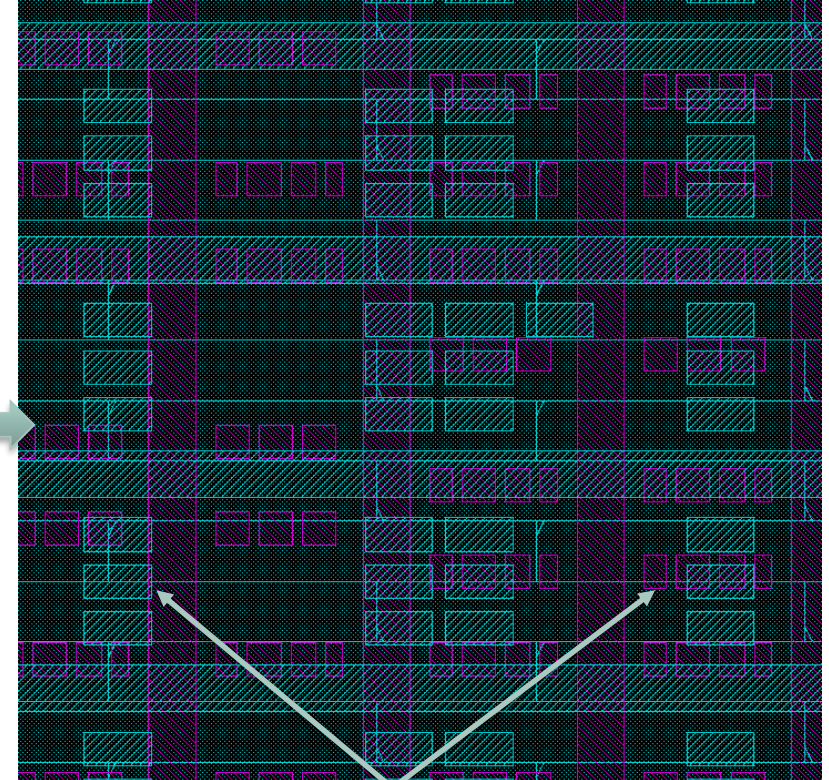
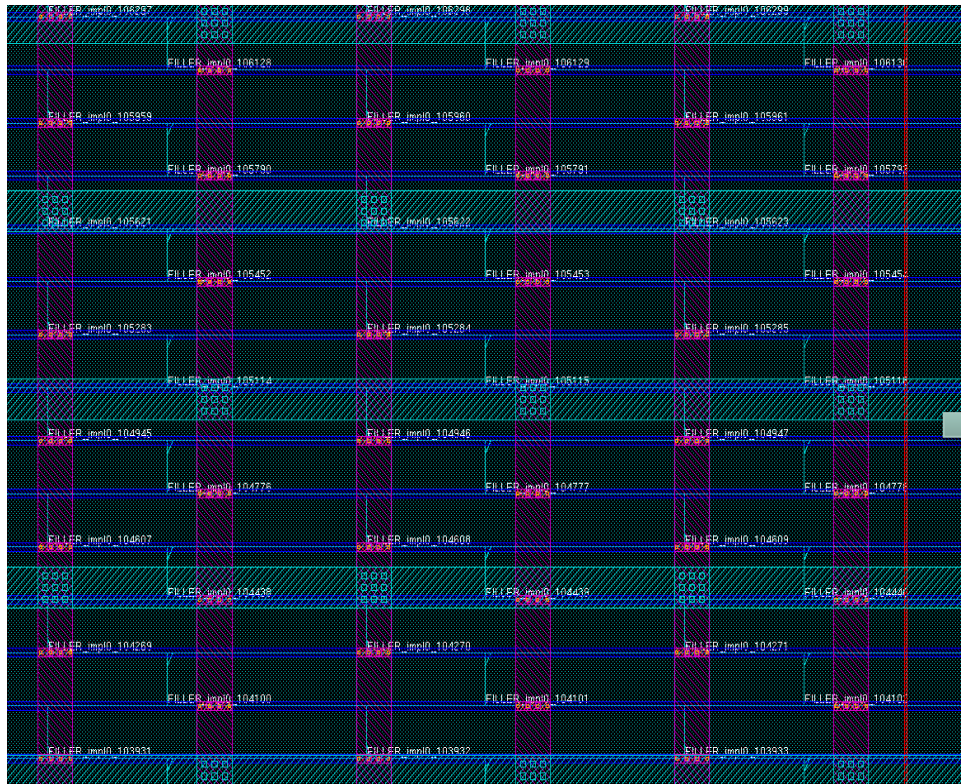
- Final Steps before manufacturing:
 - Verify and fix DRC
 - Retime/Refix design
- Perform Metal Filling to fix density DRC
 - Reverify/Retime/Refix design
- Write out a GDS file
- Perform Layout versus Schematic
 - Refix design
- Good to go!

Metal Filling

- Filling: Add Dummy metal in empty areas
- Very Important to ensure metal planarity:
 - During Metal Polishing, if the metal density is low, the isolation oxide may get polished more than the metal
 - The layer would not be planar anymore and risk damaging the next layer deposition and VIA construction
- Adds parasitic capacitance -> timing is rechecked
- Not always done in the tool, other tools can be used
- Sometimes the Foundry access service provider does metal filling (ex: Multi Project Wafer fabs)



Metal Filling



Density fillers

End Slide